Figure 4.40 shows the gain distribution. It can be seen as a Gaussian distribution with a 57.61 mV/MIP mean value and a standard deviation of $\sigma = 0.71$ mV/MIP. The two channels out of order were removed and channels 23, 33 and 39 were not considered in calculating the distribution Gaussian fitting. The channel-to-channel gain dispersion, σ, is then of the order of 1.2%. On one hand, this dispersion comes from the dispersion of the integrated component electrical characteristics. On the other hand, it comes from the cluster phenomenon described previously. One can expect that the main source of dispersion is due to the clusters. So the 1.2% dispersion can be seen as a pessimistic value. This result shows that our assumption on gain dispersion in performing the pulse generator calibration was justified.
d) Base line distribution

The base line is distributed randomly with a mean value of 296 mV and a 7 mV standard deviation, i.e. only 11.2% of one MIP as base line dispersion. Note that the base line is not disturbed by the cluster phenomenon since it is determined for 0 MIP injected.
e) Noise

For such a front-end amplifying system, the Equivalent Noise Charge (ENC) at the input is proportional to the detector capacitance. So the ENC was measured with the SSD bonded to the chip [5]. A value of 300 electrons was obtained for a detector capacitance around 5 pF. This is in the range of the specifications (< 400 electrons) [3],[4].
f) Power consumption

Until now all the measurements were carried out after biasing the circuit by the nominal currents obtained by simulation. So, for a 10 MHz readout rate, the mean power consumption per channel is given by [1]:

$$\langle P \rangle = 328 + 10^5 R_T \qquad \text{with} \qquad R_T = T_{RO}/T_C \ ,$$

where T_{RO} is the time in seconds needed for the readout of one channel (typically 100 ns at 10 MHz), the period T_C between two readout cycles is expressed in seconds and $\langle P \rangle$ is expressed in microwatts. For a typical readout cycle every 1 ms, the mean power consumption per channel is then kept to the very low value of 340 μW/channel.

4.2.2.3 Prototype module tuning

Some measurements have been performed on A128 chips connected to the detectors in the laboratory before beam tests. Using an oscilloscope to read out a selected analog channel, the pulse shape can be observed. Four analog biases (two currents: Ishaper, Ipreamplifier and two voltages: Vshaper, Vpreamplifier) control the preamplifier and shaper parameters in order to

- adjust the shaping time,
- set a stabilized polarization point of the preamplifier input stage,
- optimize the signal-to-noise (S/N) ratio.

The JTAG slow-control mechanism enables internal calibration by injection of charges in the input of a selected analog channel and tuning of four biases in order to study the amplifier output.
a) Shaper-parameter tuning

- Vshaper
  An adjustment of the Vshaper (Fig. 4.43) avoids undershoot and the output signal can be close to an ideal CR-RC. No difference in rise time is shown when the Vshaper parameter is increased. The shaping time depends only on the variation of the fall time.

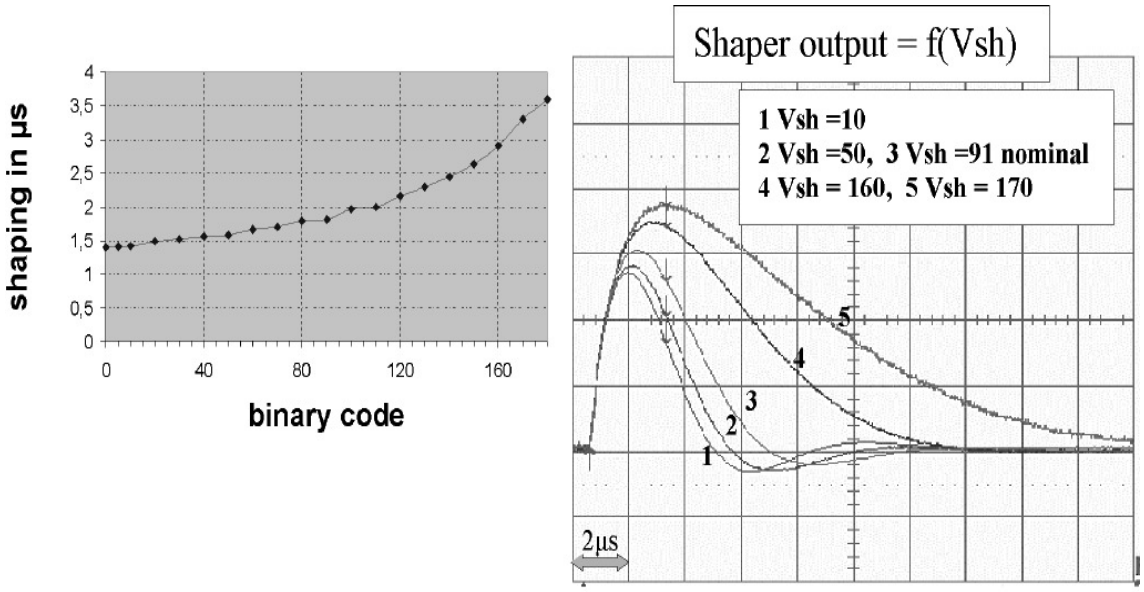

Figure 4.43: Shaping time and pulse shape when the Vshaper binary code is increased.

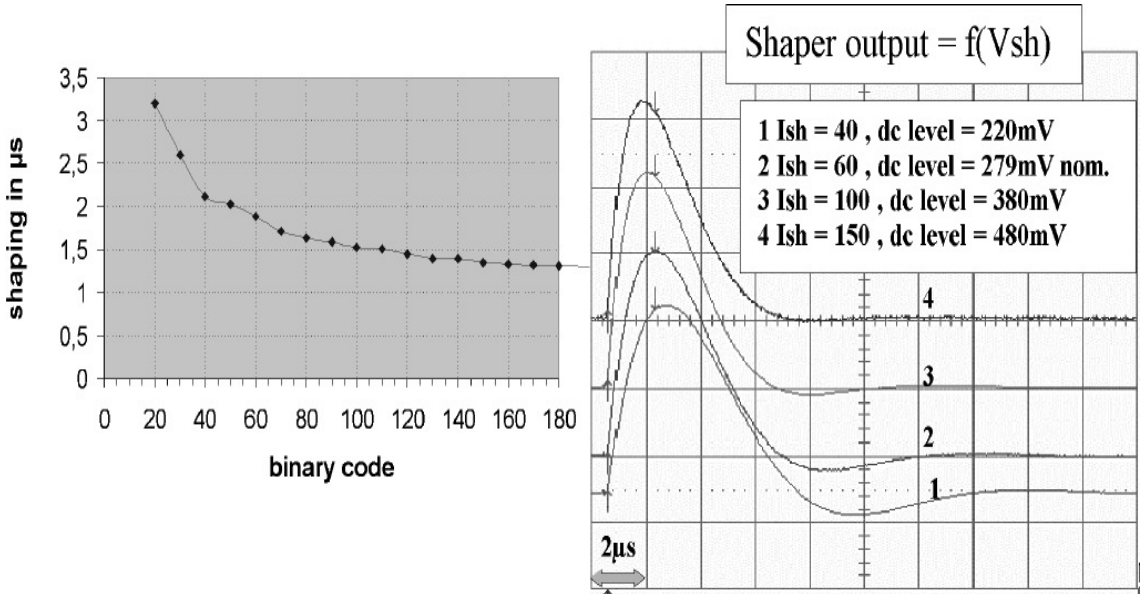

Figure 4.44: Shaping time and pulse shape when Ishaper binary code is increased.

- Ishaper
  The increase of the Ishaper (Fig 4.44) affects mainly the rise time of the output shape. The tuning of this parameter can be used for the adjustment of the DC level corresponding to the pedestal.

- Preamplifier-parameter tuning
  Figure 4.45 shows the pulse shape when the preamplifier parameters are tuned. Above the binary value Vp = 165 the pulse height decreases and a undershoot can be observed. On the other hand, when Vp is too small, an output instability can be seen, related to the big value of the feedback resistor. Adjusting Vp at the nominal value provides the optimum performance. There is no significant change of the output shape when Ip is tuned.

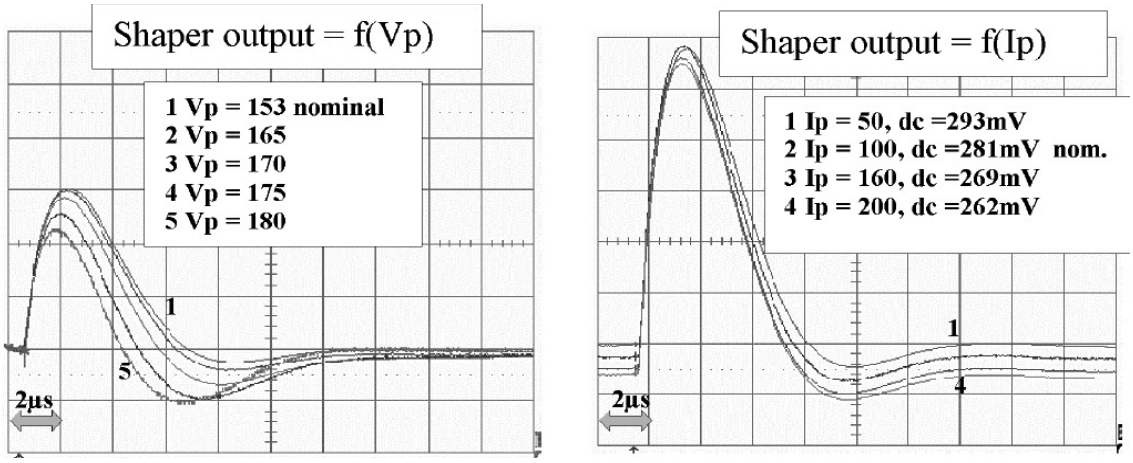

Figure 4.45: Shaper output pulse when Vp and Ip binary code is increased.

- Additional measurements with nominal parameters
  Figure 4.46 shows the output shape when the injected pulse height is increased up to ±12 MIP for shaper and preamplifier nominal parameters. The pulse shape is not dependent on the pulse height, and no variation of the shaping time is observed.

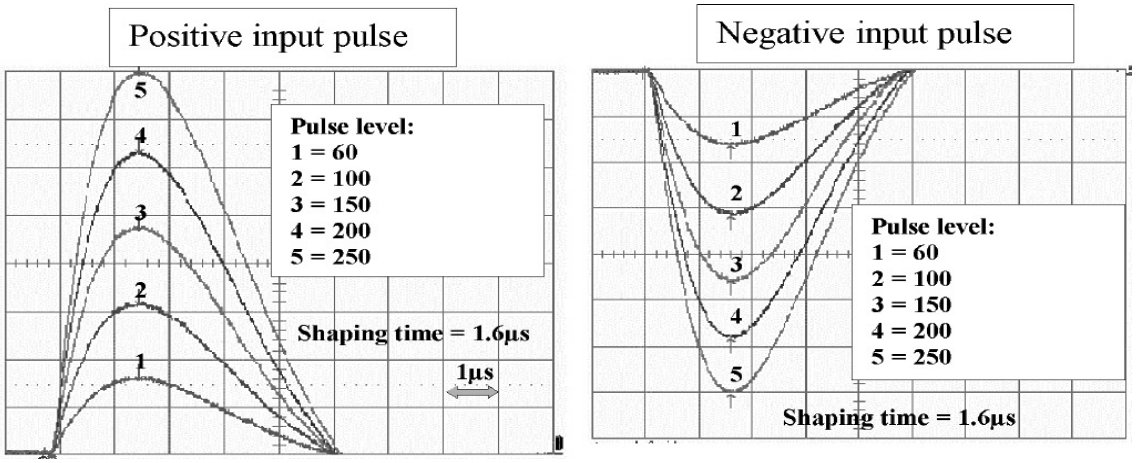

Figure 4.46: Shaper output when input pulse generator binary code is increased.

In sequential reading each channel amplifies, shapes and stores the injected charges as a voltage signal onto the C_{HOLD} capacitance. This storage is triggered by the external HOLD logic signal which comes after the triggering of the internal pulse generator.

Figure 4.47 shows the output of the shaper when the hold signal is sent and maintained. On the left side the hold signal is maintained for 1 μs. No discharge of the C_{HOLD} capacitor is observed. The right side shows the shaper output when the hold signal is maintained for 1 s. There is no significant discharge for a non-irradiated chip, but for a 20 krad irradiated chip a slope of 20 mV/s was measured and 140 mV/s for a 50 krad irradiated chip.

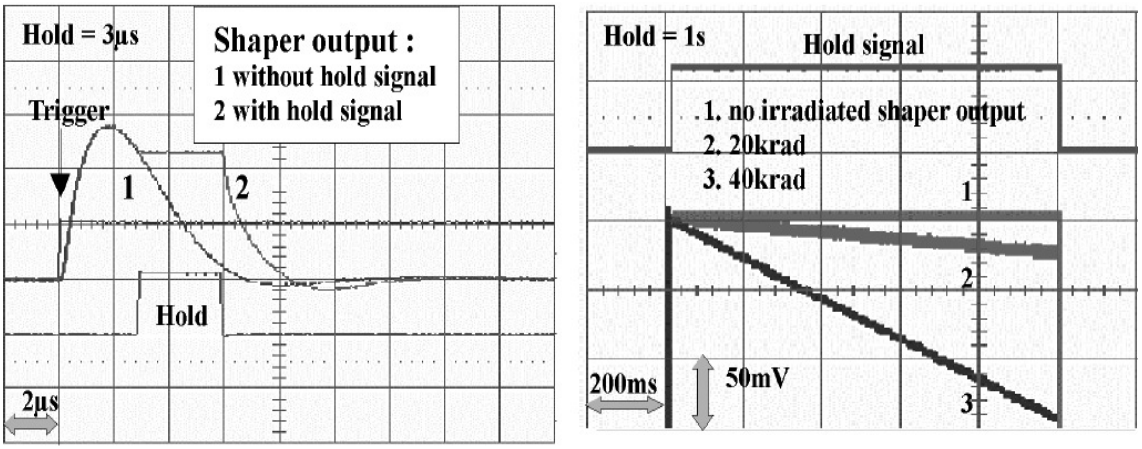

Figure 4.47: Discharge of the C_{HOLD} capacitor when the HOLD signal is maintained for 3 μs (left) and 1 s (right).

4.2.2.4 Beam-test results

The beam tests were made on different accelerator facilities: the PS and SPS at CERN (Geneva), and the Vivitron at IreS (Strasbourg). The test set-up appears in Fig. 4.48 and the results are presented in Section 4.3.

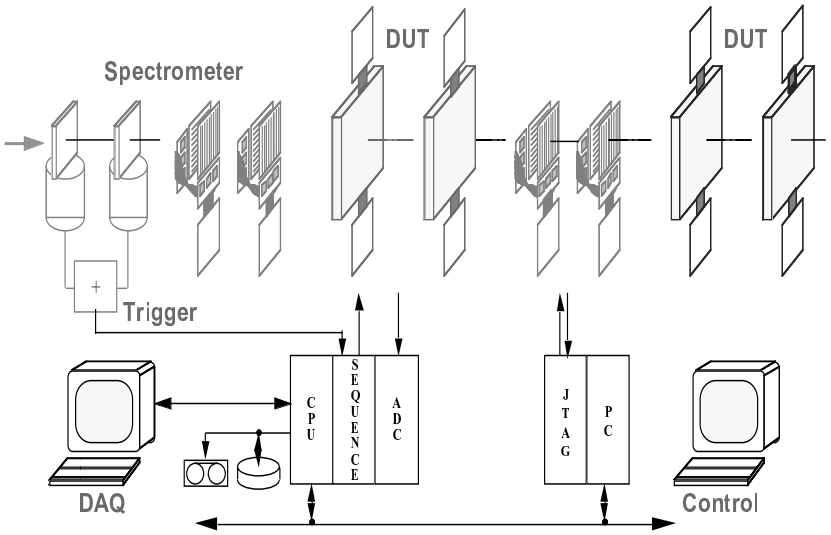

Figure 4.48: Beam-test set-up.

The results refer to the whole detector module but the noise figure study is directly correlated to the chip characteristics. The same set-up was implemented with A128C front-end chips and with the reference VA2 chips. The results concerning the noise are given in Table 4.3.

Table 4.3: Signal/noise summary for double-sided SSD

S/N	p side	n side
Detector C + VA2	55	40
Detector C + ALICE	45	40
Detector E + VA2	65	35
Detector E + ALICE	55	30

4.2.3 Chip characteristics

4.2.3.1 General data

Number of analog input channels	128
Input pitch	44 μm
Output pitch (output, power supplies, control, etc.)	136 μm
Power supply voltage	Vdd: +2 V ±0.25 V, Vss: −2 V ±0.25 V, Gnd
Absolute max. power supply	Vdd ≥ -0.3 V Vss $\leq +7$ V Vss $\leq$ Gnd $\leq$ Vdd
Quiescent power supply current	Vdd: 6 mA, Vss: 20 mA
During read out power supply current	Vdd : 25 mA, Vss: 40 mA
DC power supply rejection ratio on analog out	20 dB on base line, 20 dB on gain
Analog inputs (front end)	Directly connected to the gate of the input Pmos transistor (no ESD protection) must be AC coupled. DC quiescent voltage: −1.3 V Vss −0.3 V $\leq$ Vin $\leq$ Gnd +0.3 V
CMOS inputs	Logical 0: Vss, Logical 1: Vdd, ESD protected by diodes to Vdd and Vss Vss −0.3 V $<$ Vin $<$ Vdd +0.3 V
LVDS differential input	ΔVin $>$ 100 mV Logical 0: lowest voltage on LVDS_xxxp Logical 1: highest voltage on LVDS_xxxp
LVDS inputs common mode	from Vss +0.8 V to Vdd −0.5 V
CMOS output (Token Out)	4 mA drive capability
Tristate output (TDO)	4 mA drive capability, Ioz: ±10 μA
Analog output DC quiescent voltage	28 mV
Analog output max. output current	30 mA
Analog output saturation voltage	Vos−: −1.3 V, Vos+: +1.5 V
Analog output impedance	$<$ 10 Ω, 1.1 pF if enabled, High Z if disabled

Readout speed	$\leq$ 10 MHz
Peaking time	adjustable from 1.4 to 2 μs (at least)
Gain	60 mV/MIP (25 000 e /mip)
ENC at input	300 e for 5 pF input capacitance
Dynamic range	$\pm$355 000 e
Pedestal variation within a chip	$\sigma < 5\%$
Gain variation within a chip	$\sigma < 2\%$
Non linearity in the $\pm$5 MIP range	0.2% of full scale
Non linearity in the $\pm$10 MIP range	1% of full scale
Non linearity in the 15 MIP range	5% of full scale
Overall accuracy of the test pulse generator	better than 10%
Channel to channel variation of the test pulse generator within one chip	$\sigma < 2\%$ of full scale

Unless otherwise specified, all data are typical for Vdd: +2 V, Vss: −2 V with respect to Gnd, the shaping time adjusted to 1.8 μs and the chip loaded with $Z_l = 100\ \Omega$

4.2.3.2 Bias register values

The typical values to be set in the bias generator via the JTAG protocol (7×8 bits) are the following :

Ipreamp	100	dec
Vpreamp	153	dec
Ishaper	60	dec
Vshaper	91	dec
Iinbuff	50	dec
Ioutputbuff	100	dec
Ilvds	20	dec

4.2.3.3 Pulse level register

The amount of charge which can be injected at the input of the preamplifier is set by the value loaded in the Pulse_gen JTAG register. A value of 255 dec corresponds to approximately 15 MIP. Slight differences can be observed on the injected charge, depending on the number of test channels used. The best accuracy is obtained by testing one channel at a time in each chip. The sign of the injected charge and the timing is set by a transition on the LVDS-TEST differential input. A $0 \rightarrow 1$ transition yields a positive charge, a $1 \rightarrow 0$ transition yields a negative charge.

4.2.3.4 I/O pads

For normal operation the following rear-side I/O pads should be connected; all others should be left open.